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Reg. No. : .....

Name : .....

Third Semester B.Tech. Degree Examination, November 2013
(2008 Scheme)
08.305 DIGITAL SYSTEM DESIGN (R, F)

Time : 3 Hours Max. Marks : 100

PART – A

Answer **all** questions.

1. Perform the following conversions :

   a) FD 3.6 A to Octal

   b) $(673.62)_8$ to Decimal.

   c) $(793.75)_{10}$ to Hexa decimal

   d) $(295.75)_{10}$ to binary.

2. What do you mean by weighted code ? Give two examples.

3. Using $(\gamma-1)$'s compliment perform

   a) $(763.62)_8 - (625.73)_8$

   b) $(193.73)_{10} - (565.62)_{10}$

4. Using poster lates and theorems simplify : $f = \bar{a}bc + bc + \bar{c}$

5. Prove the following theorems :

   a) $(a+b)^{-} = \bar{a} - \bar{b}$

   b) $a + \bar{a}b = a + b$

6. What are the steps to be followed to realize a boolean function in the form of product of sum using only NOR gates ?

P.T.O.

7. Show that a full adder can be realized using two half adders. (Either show the diagram or show the proof in terms of expressions for sum and carry)

8. Discuss the working of a master slave flip flop.

9. Draw the logic diagram of a J-K flip flop using NAND gates.

10. Differentiate combinational circuits and sequential circuits. Give one example for each. **(10×4=40 Marks)**

PART – B

Answer **one** question from **each** Module

Module – I

11. a) Perform the following operations using Excess-3 code. **10**

i) 693.73 + 261.81

ii) 373.61 – 625.68

Use 10's compliment.

b) Perform the following using 8421 code. **10**

i) 4561.62 + 3915.65

ii) 291.73 – 731.23

Use 10's compliment.

OR

12. a) Perform the following using (γ -1)'s compliments. **10**

i) $(169.45)_{10}$ — $(565.73)_{10}$

ii) BCDF.6F — 93 DC.EC

iii) $(527.62)_8$ — $(721.51)_8$

iv) $(110101.101)_2$ — $(111011.100)_2$

b) Perform the following operations. **10**

i) 1101 *1010

ii) 1100 ÷ 0101

Module – II

13. a) Using 4-bit binary adders design a 8421 (BCD) adder and explain its working. 12

    b) Simplify using k-map : $f = \sum 1, 2, 3, 7, 10, 13, 14, 15$ and realize the simplified function using only NAND gates. 8

OR

14. a) Design a logic circuit using only NAND gates for converting 8421 code to excess-3 code. 12

    b) Using a 8×1 MUX realize the function. $f = \sum 1, 3, 4, 7, 9, 10, 13, 14, 15$. 8

Module – III

15. a) Give the excitation tables for JK Flip Flop and T-Flip Flop. 5

    b) Using T-Flip Flop design a modulo-10 synchronous counter. 15

OR

16. Describe briefly **any three** of the following. 20

    a) Master slave JK Flip Flop.

    b) Universal shift register

    c) Serial adders

    d) Hardware Description Language (HDL).